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Advances in surface passivation and emitter optimization techniques of c-Si solar cells

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A R T I C L E I N F O

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This paper discussed advances in several suitable passivation schemes and emitter optimization techniques available up to date. c-Si endowed with numerous crystal defects and impurities which are responsible for lower efficiency of solar cells made out of it. The surface passivations and emitter formations are the two inevitable processes to upgrade the solar cells efficiency by circumventing several induced effects due to associated crystal defects and impurities of c-Si. This work will act as a common place for the solar cell researchers, engineers and for the students to get the very recent results of surface passivation and emitter optimization techniques practiced both in the industries and R&D laboratories over the world. Key issues here to be considered while agglomerating the relevant information for each process step are the cost-effectiveness, added complexity, additional benefits, reliability, and efficiency potential.

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1. Introduction

For an easy access by all as well as to meet the grid parity with conventional electricity, solar cell needs to be cost effective. High efficiency solar cell is all that important to keep the cost at acceptable minimum. The global photovoltaic (PV) market is booming over the years. Solar cell producers have to concentrate on the cost per *Wp* of their product as the competition between the manufacturers becomes more and more important. Therefore, most cell manufacturers try to optimize their solar cell processes to gain high efficiency without any extra increase in manufacturing costs. There are four different ways to improve c-Si solar cells efficiency:

- Increased light trapping effect by improving surface structuring and texturization.
- Redistributing the emitter profile on the front surface.
- Upgrading or changing metallization processes in order to get thinner contacts with excellent electrical properties.
- Optimizing the passivation layer on both surfaces to reduce the recombination losses.

Starting from a raw wafer to until get the final cell, the solar cell has to go through different process steps. The standard process sequence for c-Si solar cell is shown in Fig. 1. Among all this stages, emitter formation and surface passivation are inevitable to culminate with a successful solar cell. Hence this study emphasized on the present status of passivation and emitter optimization of solar cells process sequences.

The surface of crystalline silicon (c-Si) represents the largest possible disturbance of the symmetry of the crystal lattice. Due to non-saturated ('dangling') bonds, a large density of defects (which is also termed as surface states) within the band gap exists at the surface of the crystal. These dangling bond defects can also be divided into intrinsic and extrinsic defects. There are typically additional processing related extrinsic surface defects as a result of dislocations, chemical residues and metallic depositions on the surface. These defects are highly prone to different recombination mechanisms namely surface recombination, auger recombination and Shockley-Read-Hall (SRH) [1.2] recombinations (occurs via defects level within the band gap). The recombination processes reduce the minority carrier life time and responsible for lower conversion efficiency of Si solar cells. One way to keep the recombination loss at tolerable minimum is to passivate the silicon surfaces electronically [3].

High efficiency silicon solar cells require both surfaces (front and rear) to be well passivated. In this regard, electrical surface passivation of crystalline silicon (c-Si) solar cells has been emerged as a key issue involving both conversion efficiency and fabrication cost. A low thermal budget (≤ 400 °C) passivation technique that remains stable against ultraviolet photons of sunlight for longer period ($\sim > 20$ years) is considered to be the more industrially convenient passivation technique.

High efficiency of silicon solar cells can also depend on the type and quality of the emitter. There are particularly standard homogeneous emitter and selective emitter available for solar cell. Among the two types of emitters, the change from a homogeneous towards a selective emitter (SE) design is high on the list. Apart from this, the development of an alternative to the fully covering Al back-surface-field (BSF) on the rear side promises higher efficiencies as well. At the moment the latter approach seems to be more difficult to realize in an industrial way for various reasons (e.g. cost, contact design, throughput, yield), therefore the realization of a selective emitter design for standard screen-printed crystalline Si solar cells is the short-term goal in industry.

In the following paragraphs, we will discuss briefly the recent developments in surface passivation and emitter optimization techniques for high efficiency c-Si solar cells. As it is not possible to get all the information free for all technologies available, this review is restricted to technologies where information is available from recent publications.

2. Technology goals and R&D issues of c-Si

Today, the vast majority of PV modules (85% to 90% of the global annual market) are based on wafer-based c-Si. Crystalline silicon PV modules are expected to remain a dominant PV technology until at least 2020, with a forecasted market share of about 50% by that time *(Energy Technology Perspectives* 2008) [4]. This is due to their proven and reliable technology, long lifetimes,

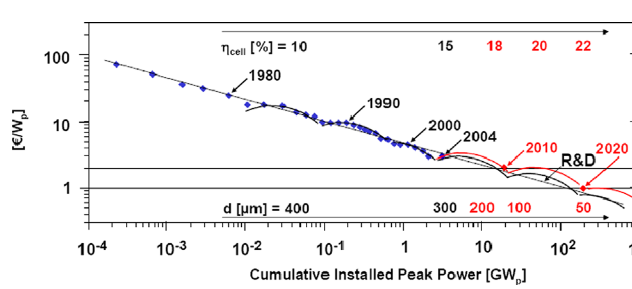


Fig. 2. Price learning curve of c-Si modules [].
source: http://www.ise.fraunhofer.de

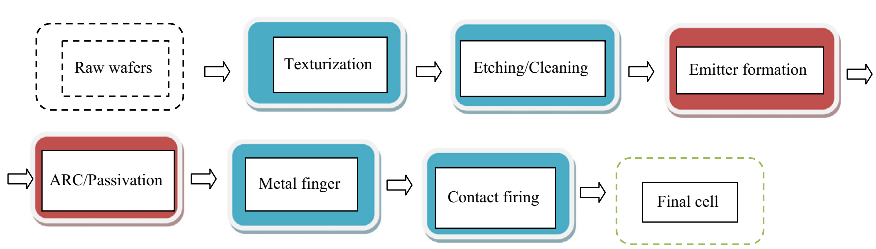


Fig. 1. Process sequences for standard c-Si solar cell.

Table 1
Goal and key R&D issues for c-Si technologies.

c-Si technologies	2010–2015	2015–2020	2020–2030/50
Efficiency targets in % (commercial modules)	Single crystalline: 21%	Single crystalline: 23%	Single crystalline: 25%
	Multi-crystalline: 17%	Multi-crystalline: 19%	Multi-crystalline: 21%
Industry manufacturing aspects	Si consumption < 5 g/watt (g/W)	Si consumption < 3 g/watt (g/W)	Si consumption < 2 g/watt (g/W)
Selected R&D areas	New silicon materials and processing	Improved device structure	Wafer equivalent technologies
	Cell contacts, emitter and passivation	Productivity and cost optimization in production	New device structure with novel concepts

Table 2
Historical development and potential of c-Si.

R&D issues	1980	2005	2020
Thickness (μm)	400	200	100
Kerf loss (μm)	400	200	100
Length (cm)	10	15	20
Efficiency (%)	10	15	20
Si [g/W_p]	30	10	3
MW_p/Line	10	100	1000

and abundant primary resources. The main challenge for c-Si modules is to improve the efficiency and effectiveness of resource consumption through materials reduction, improved cell concepts and automation of manufacturing.

Continuous targeted R&D on c-Si technologies in public and industrial research with a near-term focus can result in a substantial cost reduction (see Fig. 2) and an associated volume effect, both of which are needed to enhance the competiveness and accelerate the scaling-up of PV in the next decade. The major required R&D efforts for crystalline solar cells are summarized in Tables 1 and 2.

A list for a good number companies currently practising passivation and selective emitter techniques can be found in [5,6].

3. c-Si solar cell surface passivation techniques

An excellent electrical interface quality is essential for many devices relying on the bulk electronic properties of semiconductors [7]. Electrical losses at a semiconductor interface or surface should be minimized in photonic devices based on group III–V or group IV semiconductors when radiative recombination should be the dominant process [8,9]. Moreover, electronic losses at the crystalline Si (c-Si) surface have become increasingly important in the field of c-Si solar cells due to the trend toward thinner c-Si wafers used as base material. Consequently, the reduction of recombination losses at semiconductor interfaces is a prime concern for numerous semiconductor applications.

Recombination losses at a semiconductor interface or surface can be reduced by two different passivation strategies. The first strategy is based on the reduction in the number of defect states at the interface. The interface defect density can be reduced significantly by the passivation of undercoordinated atoms (dangling bonds) by, e.g., atomic H or by a thin dielectric or semiconductor film. This strategy is commonly referred to as chemical passivation. For example, the mid gap interface defect density of c-Si can be as low as $10^9\,eV^{-1}\,cm^{-2}$ after the growth of a high quality thermal SiO_2 film and a subsequent anneal in a H_2 atmosphere, e.g., a forming gas anneal [10].

The second strategy is based on a significant reduction of the electron or hole concentration at the semiconductor interface by means of a built-in electric field. Recombination processes is the interaction between electrons and holes. The highest recombination rate is obtained when the electron and hole concentration at the interface are approximately equal in magnitude (assuming identical capture cross sections for electrons and holes). In other cases the recombination rate scales with the minority carrier concentration at the surface. In the so-called field-effect passivation, the electron or hole concentration at the semiconductor interface is altered by electrostatic shielding of the charge carriers through an internal electric field present at the interface. This internal electric field can either be obtained by a doping profile below the interface or by the presence of fixed electrical charges at the semiconductor interface. Consequently, the application areas of field-effect passivation are limited but the effect can be employed successfully in devices such as light emitting diodes and solar cells.

There are two fundamentally different types of surfaces in a c-Si solar cell: metallised and non-metallised surfaces. Metal silicon interfaces feature very high surface recombination velocities and need to be carefully designed to avoid excessively large recombination losses. Similarly, in order to ensure a good blue response of the cell, the illuminated non-metallised surface regions (i) need to be well passivated and (ii) not too heavily doped to avoid the formation of a dead layer. In the case of laboratory c-Si cells, the importance of the passivation of both cell surfaces is well recognized. Recent advances in the c-Si surface passivation methods (as best of our knowledge) are enumerated below.

3.1. Front surface passivation

Thermal growth of silicon oxide is the most effective c-Si surface passivation technique for solar cell. As it requires very high temperature (above 1000 °C) treatment, this technique is not suitable for low-cost industrial processes. High temperature degrades the bulk life time significantly as well as the stability of passivated surface [11]. In the last two decades, various research efforts have been devoted to the development of a more industrially convenient solution, in particular, on passivation layers deposited at low temperature (≤ 400 °C) onto the c-Si surface. SiN_x front side passivation using Plasma Enhanced Chemical Vapor Deposition (PECVD) has been evolved as an alternative to high temperature oxidation of silicon [12–14]. Record low effective surface recombination velocity (SRV) of 4 cm/s has been obtained on 1 Ω cm p-Si wafers for SiN_x using remote PECVD or high-frequency (13.56 MHz) direct PECVD [13]. SiN_x passivation for front surface of c-Si solar cells is deemed to be superior over other passivation techniques such as SiO_2, TiO_2 etc. due to its (i) field effect passivation provided by positive interface charges, (ii) properties of capture cross-sections of dominant defects, (iii) adjustable refractive index as antireflection coating (ARC) and (iv) hydrogenated passivation of bulk defects [5,11,15,16].

3.2. Rear surface passivation

Using thinner wafers and an effective reduction of surface recombination losses are increasingly important for low-cost highly efficient silicon solar cells. Hence the recent trend in silicon-wafer-based PV

industries is toward thinner wafers (< 200 μm). But use of thinner wafers increases the rear surface recombination [11]. Thus the use of thinner wafers necessitates a well passivated rear surface to keep the rear surface recombination loss in acceptable minimum. Moreover, the increasing demands for optical quality require a higher internal reflection. Therefore, all designs for high-efficiency silicon solar cells today use a dielectric passivation layer on the rear to meet the requirements of passivation quality and optical properties. Keeping in mind the above attributes a good number of rear surface passivation techniques were developed over the years, among them ALD assisted Al_2O_3, wet oxidation process using pyrogenic steam, passivation by stack of a-Si:H/SiO_2 or Al_2O_3/SiN_x and passivation by Phosphorus-Doped a-SiC_xN_y:H(n) alloys are the most notable rear side passivation techniques for crystalline silicon solar cells. Recent research results on these rear surface passivation techniques are aggregated below.

3.2.1. Rear passivation by Al_2O_3

In the case of mc-Si wafers, thermal processes above 900 °C typically lead to a significant degradation of bulk lifetime [17]. Al_2O_3 rear passivation by atomic layer deposition (ALD) has been evolved as an alternative of low-temperature surface passivation for high efficiency silicon solar cells which have comparable properties as that of the alnealed SiO_2. Using low-temperature plasma assisted ALD, SRVs of < 13 cm/s were demonstrated on low-resistivity p-type c-Si [18]. A detailed study on ALD deposited Al_2O_3 has been reported in [19] by J. Schmidt et al. The excellent passivation of low-resistivity p-type silicon by negative-charge-dielectric Al_2O_3 was confirmed on the device level by an independently confirmed energy conversion efficiency of 20.6%, a V_{oc} of 660 mV and a J_{sc} of 39.0 mA/cm^2. Moreover, Al_2O_3 passivation overcomes the so called 'parasitic shunting' effects [20] which is very common for SiN_x passivated rear.

3.2.2. Wet oxidized rear passivation

A wet oxidation process using pyrogenic steam [21] at 800 °C has been applied on 250 μm thick boron-doped (0.5 Ω cm) high quality Float Zone (FZ) silicon to study its suitability for rear side passivation at Fraunhofer ISE [22]. The study focused on the determination of the benefit of the point-contacted oxide passivated rear compared to the full area Al-BSF. In the long wavelength region of incident photons, this wet oxidized rear passivation has high internal reflectance which leads to an absolute gain of 6% in J_{sc} and V_{oc} compared to Al-BSF cells though there is about 3% absolute loss in FF due to increase in series resistance for point-contacts [23]. Their experimental results also showed an effective carrier life time of 35 μs and surface recombination velocity (SRV) of ≤ 38 cm/s for silicon wafers [22]. In addition, this wet oxidation process has about one order of magnitude faster growth rate than the traditional high temperature (1050 °C) dry oxidation process [24] and can close the gap between laboratory and industrial application by overcoming the longer high thermal budget of dry oxidation.

3.2.3. Rear passivation by stack of a-Si:H/SiO_2

Rear surface passivation by stacks consisting of a-Si:H and SiO_x on boron-doped p-type FZ wafers (0.5 Ω cm) with shiny-etched surfaces were examined at Fraunhofer ISE [25,26]. By using this passivation layer system at a solar cell's rear side, surface recombination velocity below 10 cm/s on 1 Ω cm p-type Si wafers and the best achieved energy conversion efficiency of 21.7% (that was confirmed by the Fraunhofer ISE CalLab) was reported in [25]. More importantly, it is a low-temperature (200–400 °C) passivation technique. Experimental results showed a steady increase in the open-circuit voltage, V_{oc} from 645 mV to 676 mV and in the short-circuit current density, J_{sc} from 38.5 mA/cm^2 to 39.3 mA/cm^2 for a change in temperatures from 200 °C to 400 °C. However, the stability of the above mentioned performances of this passivation technique in a standard firing process (800–850 °C) could not be achieved [25].

3.2.4. Passivation by phosphorus-doped a-SiC_xN_y:H(n) alloys

Amorphous silicon nitride (a-SiN_x:H) deposited by PECVD was prevailed as the most feasible alternative to thermally grown silicon oxide on c-Si surface due to its ability to serve as both passivation and anti-reflection coating. Recently, a study conducted on amorphous silicon carbide (a-SiC_x:H) proved that it could be the best alternative to a-SiN_x:H [13,27]. Its optical characteristics can be tuned by the carbon content of the film. Phosphorus-doped amorphous silicon carbide (a-SiC_x:H(n)) demonstrated the ability to passivate p-type c-Si substrates [28–30] and highly doped n-type emitters in solar cells [31]. Very silicon-rich films yielded effective surface recombination velocities at 1 sun-illumination as low as 3 cm/s and 2 cm/s on 1 Ω-cm p- and n-type crystalline silicon substrates, respectively [32]. An efficiency of 20.2% was reported for passivated emitter rear cell (PERC) [26] following the approach in [31].The reported values were obtained without forming gas alneal (FGA). The stability in surface passivation was verified for a 2-month period. Such stacks have the additional benefit of being more dielectric than silicon-rich films, thus avoids the degradation of field effect passivation due to shunting effects [20].This result demonstrates that a-SiC_xN_y:H(n) films can be useful for designing high efficiency c-Si solar cells.

3.2.5. Passivation by Al_2O_3/SiN_x-layer stack

To study the effectiveness of rear passivation by the stack consisting of Al_2O_3 /SiN_x, recently the large area wafers (125 × 125 mm^2) were coated with 15 nm of Al_2O_3 and with 80 nm of SiN_x at University of Konstanz [33]. The Al_2O_3 layer was deposited in an Oxford FlexAL and the SiN_x in an industrial direct plasma PECVD reactor. The operating temperature of the PECVD system was slightly adjusted to offer ideal annealing conditions for Al_2O_3 according to [18]. Despite the merits of Al_2O_3, it was shown that the samples which are passivated by a single layer of Al_2O_3 without the protecting SiN_x layer show a largely destroyed Al_2O_3 layer after metallization etch-back [33]. Investigations on lifetime samples showed a 2.5-fold increase in effective lifetime and an efficiency gain of 0.7% absolute (max. efficiency 18.6%) for surfaces passivated by an Al_2O_3/SiN_x stack compared to fully metallized Al-BSF rear sides. An increase in the infrared spectrum of the internal quantum efficiency is determined as the source of this gain. However, this cell exhibited a reduction in FF due to an increase in series resistance locally. It was claimed that this particular passivation technique is industrially feasible [33].

3.2.6. Efficiency comparison of different passivation techniques in cells level

Aggregated results of efficiencies of different cell types after exploiting different passivation schemes are shown in Table 3.

4. Emitter optimization

Emitter formation is the very basic step of solar cell process sequences. The higher conversion efficiency of a solar cell much more depends on the type and quality of the emitter. There are two types of emitters are currently under practice both in industries and in laboratories. One is conventional homogeneous emitter that is formed over the whole surface area of the silicon wafer, and other is selectively doped emitter.

Table 3
Surface passivation methods of c-Si solar cells that were developed in the last 30 years. (Efficiencies shown in the table are the theoretical limit).

Cell concepts/types	Types of passivation used	Merits of passivation used	Demerits of passivation used	Efficiency (%)	Ref.
Screen-printed cells	p–n Junction passivation	Robust, reliable and low cost, high V_{oc}	Larger shading loss, poor blue response, modest short-circuits currents	15–16	[3,11]
Buried-contact cells	Thermal oxide passivation	Low recombination and resistive losses. Reduced shading loss by 50%	High temperature process, degrade bulk lifetime	17–18	[3,11]
PERL/LBSF cells	Thermal oxide passivation	Lower surface recombination	High temperature process, degrade bulk lifetime	24.7	[3,11]
Backside-contact concentrator solar cells	Thermal oxide passivation	Eliminate metal shading loss, facilitating the interconnection of individual cells	High temperature process, degrade bulk lifetime	22.7–26	[3,11]
Bifacial cells	Silicon nitride passivation	Both surfaces of the cell are passivated, minimize reflection losses etc	High temperature process	18.1–20.1	[3,11,12–14]
MIS inversion-layer cells	Silicon nitride passivation	Low temperature treatment, promising candidates for cost-effective generation of PV electricity	High temperature process	18.5	[3,11,12–14]
HIT cells	Double-layer stack of a-Si	Low SRV, junction is formed at only 200 °C	Stable performance could not be achieved at higher temperature	20.0	[3,11,25,26]
Thin-film polycrystalline silicon cells	PECVD deposited silicon of only 2 μm	Very thin, low cost	N/A	10.1	[3,11]

A significant reduction in the production costs of solar cells can be achieved mainly by two ways, either by decreasing the thickness of the wafers or by increasing the cell efficiency. The latter can be achieved with selective emitter solar cells, which can be manufactured by screenprinting of dopant pastes in industrial mass production. During emitter formation efficient gettering of impurities is essential to improve the wafer quality as these impurities lead to unwanted Shockley-Read-Hall (SRH) recombination.

Some of the recent advancements in emitter optimization to achieve higher conversion efficiency are ascribed here.

4.1. Full area emitter formation

Solar cell efficiency of 18.4% on CZ- large area cells following standard solar cell processes was reported in [34] for full area homogeneous emitter. Further optimization of this homogeneous emitter approach required the development of such pastes that can contact the emitters with higher sheet resistance R_{sheet} [35] and/or the so-called seed-and-plate approach where a paste optimized for contacting high R_{sheet} emitters is used as a seed for an additional plating step which provides very good grid conductivity [36].

4.2. Selective emitter formation

On today's industrial type solar cells the front side is homogeneously doped to a level of typically 50 Ω/sq which is a compromise between emitter performance and sufficiently low contact resistance [37]. This compromise can be overcome by a selective emitter (SE). The SE is normally formed by heavily doped the underneath of the contact grid and by weakly doped in the illuminated area. This leads to a reduced contact resistance as well as lower Auger- and SRH recombination; hence results in improved blue response and a higher open circuit voltage. For successful implementation of a selective emitter process into industrial mass production, several aspects have to be considered such as— (i) a minimum of extra steps (ii) possibility of implementation into existing cell lines (iii) no yield losses (high stability and reliability) (iv) higher efficiencies (also for mc Si) (v) higher efficiency not only on cell but also on module level. As a rule of thumb, efficiency should be increased by 0.2% absolute for every extra step needed [34]. Several SE technologies have developed within the last few years for the purpose of implementation in industrial mass production. In this section, several of them are presented, with the restriction to those which are already in production (or close to) and where recent published academic information is available.

4.2.1. Etch-back emitter

The etch-back process can be realized with high homogeneity on large area wafers by forming porous silicon in a wet-chemical solution and removing the porous silicon afterwards [38]. Etch-back emitters can decouple the emitter saturation current densities and sheet resistances to a certain degree. The phosphorous concentration on the surface can be lowered while the emitter depth is still sufficient to reach a good lateral conductivity. This high efficiency selective emitter is suitable for a screen printing metallization process, and the finger distance can be chosen wide enough to not increase shading losses [39].

First published results [38] using 5 in. Cz–Si wafers (1.5 Ω-cm) showed an efficiency increase of 0.3% absolute compared to reference cell with homogeneous emitter. The efficiency of 18.7% for the solar cell employing the etch-back selective emitter was confirmed by FhG-ISE CalLab (stable efficiency under illumination). By changing the initial $POCl_3$ diffusion to 20 Ω/sq and etching back to 95 Ω/sq, a maximum efficiency of a selective emitter solar cell was measured to 19.0% [39].The etch-back process in combination with a masking step is an industrially feasible scheme to form a selective emitter structure on p-type wafers. This process has already commercialized by Schmid [34].

4.2.2. Inline selective emitter concept-INSECT

In recent years the concept of in-line processing has become more attractive with different techniques emerging, suitable to replace methods requiring the handling of large batches of wafers. An inline diffusion system usually consists of a doper that coats the wafers with a defined amount of phosphorus containing dopant before they are transported through a conveyor belt furnace in a controlled ambient at standard pressure.

Applying inline selective emitter concept, an increase in V_{oc} by 18.6 mV and an increase in J_{sc} by 1.2 mA/cm^2 were obtained followed by an average efficiency gain of 1.4% and a fill factor (FF) improvement by 1.3% compared to homogeneous inline emitters [40]. The improved FF originated from the choice of a higher doping level beneath the grid fingers. The rise in open circuit voltage comes from the better emitter saturation current. This means that less Auger recombination takes place in the

Table 4
I–V results for SE technologies (B-doped Cz, full Al-BSF). Given are best cell *I–V* parameters [34].

SE technology	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF (%)	η (%)	Size [mm]
Etch-back	640	**37.9**	78.4	**19.0**	125/156
Laser doping (P-glass)	637	37.0	78.9	18.6	156
Laser doping (LCP)	633	37.3	**80.3**	**19.0**	156
Laser doping (P-acid)	639	37.8	77.8	18.8	156
Si ink	637	37.5	79.0	18.9	125/156
Oxide diffusion mask	634	37.2	79.2	18.7	156
Ion implantation	**643**	37.3	78.4	18.8	156

emitter region. An increase in the overall charge carrier lifetime has resulted due to less Auger recombination. Consequently, the larger number of unhampered carriers allows their quasi-Fermi-levels to spread further. As a result, we have an increase in V_{oc}. On the other hand, the rise in current density originated from the better blue response of the emitter due to absence of the so called 'dead layer' (which is the topmost layer of the emitter containing very high quantities of phosphorus in the range of 10^{21} cm^{-3}). Short wavelength photons (i.e. photons of blue ray of sun-spectrum) cannot penetrate silicon very deeply and are usually absorbed within the emitter region [41,42].

Moreover, the in-line doping technique overcomes the intricate and complex handling of large number of wafers by so called batch process, results in less wafer breakage, and offers an excellent stable doping homogeneity.

4.2.3. Add-on laser tailored selective emitter

An add-on laser tailored selective emitter process [43] developed and patented by Institute of Physical Electronics (IPE), University of Stuttgart. This particular scanned laser doping add-on process avoids the complex masking steps for selective diffusion [44] or emitter etch back [40] and hence is very compatible for industrial mass production as well as in a research environment [7]. This patented laser doping process for SE could be realized by using a pulsed Nd:YAG laser with 532 nm wavelength, 20 kHz pulse repetition rate, and 65 ns pulse duration having a Gaussian beam shape which melts the wafer surface locally and enables the fast incorporation of phosphorus atoms from the PSG-layer, up to 800 nm deep into the molten silicon within a few hundred nanoseconds. The molten silicon cools, re-crystallizes epitaxially, and forms a highly phosphorus doped selective n-type emitter without incorporation of any grain boundaries and dislocations [45].

Applying this add-on laser doping process for SE emitter formation on 170 μm thick, p-type CZ wafers of 12.5 cm × 12.5 cm in size, an efficiency gain of 0.5% absolute is obtained [46]. The ipeLD process reached a record solar cell efficiency of 18.9% [45]. It had reported that the increase in gain by 0.5% results from a higher short circuit current, J_{sc} and an improved open circuit voltage, V_{oc} due to less auger recombination and better blue response. The reported value for J_{sc} is 37.1 mA/cm^2 and for V_{oc} is 629 mV [7]. This technology adds only one extra step in industrial process line of silicon solar cell fabrication, and is commercialized via Manz [34].

4.2.4. Laser doped SE via LCP/plating

The Fraunhofer ISE developed a SE approach which is based on simultaneous ablation of the PECVD SiN_x layer and melting of the emitter layer underneath the ablated region (~120 Ω/sq) using a liquid-guided (liquid contains P-atoms serving as P-source) laser beam (laser chemical processing, LCP) [47]. Only one extra step is added and plating allows for thinner, highly conductive grid lines compared to screen printed contacts.

University of New South Wales (UNSW) developed a process similar to the one described above. Instead of the LCP the doping source can be phosphoric acid deposited on the wafer prior to laser doping. Two extra steps are added and the approach allows for thinner, highly conductive grid lines as well. Roth and Rau are working on commercialization of this technique [48].

4.2.5. Doped Si inks

Innovalight Inc. developed a technology based on highly doped Si nano-particles which can be deposited onto the Si wafer surface via screen-printing prior to P-diffusion [49]. Hereby the ink is deposited only in the areas where the screen-printed front contact is located afterwards. In the following P-diffusion step a lowly doped emitter is realized in the uncovered areas (80–100 Ω/sq) whereas the areas with the highly doped Si nano-particles serve for contacting (30–50 Ω/sq). This technology adds only one additional step to the cell process prior to P-diffusion

4.2.6. Oxide mask process

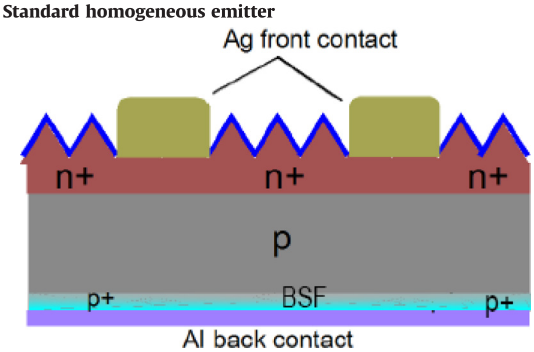
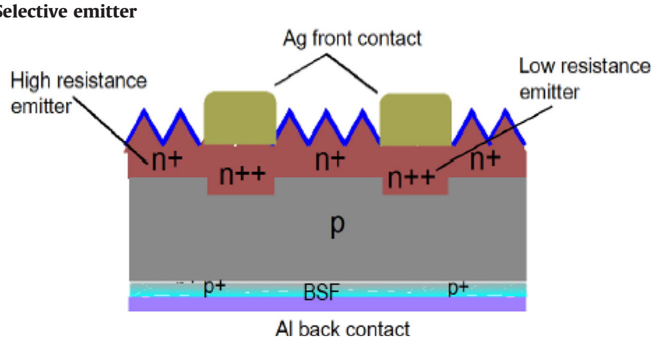
Centrotherm presented a SE technology based on a masked P-diffusion, where a thin SiO_2-layer slows down the diffusion of P-atoms from the surface into the Si bulk underneath the SiO_2 [50]. The structuring of the SiO_2 is done via laser ablation of the areas where the contacts are formed afterwards. A wet chemical etching step removes the damage induced by the laser. The heavily doped region (300 μm wide) results in 45 Ω/sq and the masked area in 110 Ω/sq. This technology offers a certain degree of freedom in emitter formation and uses technologies already established in PV. Their recent results shows the cell efficiencies up to 19.5% for a rear side passivated and locally contacted solar cells with laser diffused SE. This new technology enables the advanced rear side optical reflection and electrical passivation in combination with a blue responsive front side emitter with a reasonable gain in short circuit currents and in the open circuit voltages as well [51].

4.2.7. Ion implantation process

In ion implanted selective emitters, all doped areas have been produced by ion implantation. The innovation in manufacturable technologies that can enable higher cell efficiency at lower cost is required to meet the grid parity. Solar cells made by ion implantation reduce the fabrication complexity, number of processing steps and cost, and might provide an opportunity to attain the grid parity goal. Ion implantation scheme reduces the number of process steps from nine to eight as compared to the widely practiced $POCL_3$ process. The independently tested and validated by Fraunhofer ISE, an absolute gain of 0.8% in efficiency is possible relative to $POCL_3$ cell by ion implantation scheme [52]. This improvement in efficiency is attributed to better dopant uniformity at higher sheet resistance, tailoring profiles for reduced emitter recombination, the ability to passivate with thermal oxide, excellent screen printed contacts to the ion implanted emitter, the elimination of PSG etch and edge isolation, formation of boron BSF to replace Al BSF to enable thinner and less expensive wafers, and formation of B doped emitter and P doped front or back surface fields to enable n-type front and back junction cells with no light induced degradation [52,53].The highest efficiency ion implanted solar cell that has been reported to date is 20% for interdigiated back contact (IBC) solar cell [54].

Varian recently introduced a new technology for selective emitter formation (Solion Blue) based on ion implantation through a mask which reduces the implanted dose in the areas between the contacts [55,56]. An annealing step in oxidizing ambient is carried out for crystal damage removal caused during implantation

Table 5
Merits and demerits of emitter formation's techniques [Ref. 34, 35, 37].

<table>
<tr><th>Name of the emitter</th><th>Merits</th><th>Demerits</th></tr>
<tr><td>Standard homogeneous emitter

</td><td>• Better contact with metal fingers</td><td>• Poor blue response (Low I_{sc})
• High contact resistance (Low FF)
• High reverse saturation current (Low V_{oc})
• Narrow process window for contact firing</td></tr>
<tr><td>Selective emitter

</td><td>• Improved blue response
• Low reverse saturation current
• Low series resistance</td><td>No information available yet.*</td></tr>
</table>

* Selective emitter emerged as the solution of the problems of homogeneous emitter.

Table 6
Deployment of SE techniques in mass level (Commercial use).

SE techniques	Name of the industry use it	References
Etch-back emitter	Scmidt, Germany	[34]
Laser doped emitter	Manz,Germany, Roth and Rau, Netherlands	[37,42]
Doped Si inks	Innovalight Inc., USA	[49]
Oxide mask process	Centrotherm, Germany	[50]
Ion-implanted emitter	Varian, USA	[55]

and forms a thin SiO_2-layer on the wafer surface, which acts as surface passivation. The process continues with SiNx:H deposition. Advantages of this approach are the dry processing for emitter formation, the lack of P-glass formation (which normally has to be removed) and of junction isolation. In addition, the amount of process steps is not increased.

Besides the associated merits, ion implantation poses several challenges and demand in-depth understanding and control of ambient condition, wet chemistry, interaction between energy, dose and anneal conditions, doping profiles and bulk lifetime etc. Otherwise, lots of secondary effects can arise that might be very detrimental to ion implanted cells [52].

4.2.8. Experimental results of SE technologies

There are many critical issues that should be considered when results of the different SE technologies are compared. Some of them are differing cell formats, different *I–V* testers with different calibration cells, Ag/Al pads on the rear side, differing wafer resistivities, and Measurement before or after BO-related degradation (Cz Si)

Nevertheless, some conclusions can be drawn from the results given in Table 4. The first striking fact is that the potential of all approaches reached so far seems to be very similar. For the best cells efficiencies are in the high 18% range, with typical values of J_{sc}=37.5 mA/cm^2, V_{oc}=640 mV, FF=79% limiting efficiency to η=19.0%. For the laser doping via LCP and phosphoric acid front contacts are fabricated by plating whereas for all other technologies standard Ag screen-printing was applied. The different technologies might not necessarily be totally optimized yet, but the main limitation for the *I–V* parameters is the full Al-BSF at the rear side. Interestingly, first average efficiency data from industrial mass production lines and from pilot line processing at the equipment manufacturers seem to be very similar as well. Again, further optimization may lead to higher average values as well. Compared to the efficiency potential of around 18.4% for a Cz Si solar cell with homogeneous $POCl_3$-emitter using standard industrial-type processing an efficiency increase of 0.5–0.6% absolute is achieved with a selective emitter structure and the full Al-BSF as rear side contact [34].

4.2.9. Comparison of emitter formation techniques

A comparison of standard homogeneous emitter and selective emitter techniques has shown in Table 5.

The selective emitter techniques that are currently practicing in industry for mass production are enlisted in Table 6.

5. Discussion on surface passivation and emitter optimization

c-Si solar cell showed highest penetration in PV markets due to (i) comparative lower price of silicon wafers and (ii) the facility of due exploitation of long established technology for silicon based microelectronics. The dark side of wafers made out of silicon is its lower minority carrier lifetime. One of the main reasons for lower

lifetime is the presence of surface states due to unsaturated bonds between adjacent atoms in Si crystal. By passivating the surface states, an augment in carrier lifetime to a greater extent is proved experimentally. Hence, the surface passivation evolves as a promise for high efficiency silicon solar cell. A low temperature but stable surface passivation is very desirable for low cost high efficiency solar cell. Among several alternative have been quested so far, atomic layer deposited Al_2O_3 shows the best results for silicon surface passivation. More research endeavour needs to get an ultimate surface passivation technique which is low cost, stable and effective at low temperature.

The emitter area is the region that emits or injects most of the charge carriers under dark operation. A good emitter should has the attributes of better internal quantum efficiency for short-wavelength light, low-loss lateral transport of majority carriers from the location where they are collected to nearby metalized area, and maximum output voltage by optimum doping concentration [57]. A low resistance, low Auger recombination and high carrier collection efficiency are all that important for an efficient emitter. Among several approaches, selective emitter is very close to meet those demands.

6. Conclusions and outlook

Every c-Si solar cell fabricated to date features one or more of the surface passivation methods. With regard to solar cell applications, it is important to make sure that the surface passivation is long-term stable (> 20 years) and stable against the UV photons of sunlight. Possibly, a standalone category for rear-passivated LFC c-Si cells may emerge, but the prevailing thought remains that rear-surface changes will form incremental improvements to the advanced c-Si cell types with timelines dictated by industry-wide trends governing the introduction of wafers with thicknesses below ~160 μm.

The full potential of selective emitters with their low emitter saturation current values can be exploited when improved rear side concepts will be available for industrial application. The big game changers right now within the c-Si segment come under the heading of "selective emitter"—a somewhat generalized term that actually encompasses varying approaches (and process flows/production tooling) toward the same end goal. Selective emitters provide an immediate efficiency boost to the standard c-Si cell type, anywhere from 0.3% to > 2% depending on other efficiency-enhancement steps implemented alongside (improved passivation, metallization, etc.).

Solar cells made from crystalline silicon have lower conversion efficiency, hence optimization of each process steps are very important. Increasing the efficiency of crystalline silicon solar cells relies on the understanding and optimization of each individual processing step and the interplay between the material properties and the processing conditions. The focus of this article was to review the recent advances in existing surface passivation and emitter optimization techniques in an industrial process line as well as in the research laboratories over the world. However, while needed modification of any fabrication process, it must remember that the amount of extra steps should be kept to an absolute minimum and the general cell line concept should not be changed drastically to make the approach cost-effective and easy to implement.

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